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An Ultrafast Nonvolatile Memory with Low Operation Voltage for High-Speed and Low-Power Applications

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Memory plays a vital role in modern information society. High-speed and low-power nonvolatile memory is urgently demanded in the era of big data. However, ultrafast nonvolatile memory with nanosecond-timescale operation speed and long-term retention is still unavailable. Herein, an ultrafast nonvolatile memory based on van der Waals heterostructure is proposed, where a charge-trapping material, graphdiyne (GDY), serves as the charge-trapping layer. With the band-engineered heterostructure and excellent charge-trapping capability of GDY, charges are directly injected into the GDY layer and are persistently captured by the trapping sites in GDY, which result in an ultrafast writing speed (8 ns), a low operation voltage (30 mV), and a long retention time (over 10^4 s). Moreover, a high on/off ratio of 10^6 is demonstrated by this memory, which enables the achievement of multibit storage with 6 discrete storage levels. This device fills the blank of ultrafast nonvolatile memory technology, which makes it a promising candidate for next-generation high-speed and low-power-consumption nonvolatile memory.

1. Introduction

As an important component of computer, numerous memory technologies including static random-access memory, dynamic random-access memory (DRAM), and flash memory have been developed in the past four decades,[1] greatly promoting the development of integrated circuit industry at the pace of Moore's low. Nowadays, memory technology is facing severe challenges as the gap of data-processing speed between processors and memories, i.e., "memory wall," continues to grow larger, which seriously restrain the computing performance.[2–4] The volatile memories such as DRAMs feature an ultrahigh operation speed (1–10 ns) but a limited retention time on the millisecond timescale, whereas the nonvolatile memories exhibit excellent retention characteristics but a relatively slow speed (slower than 100 µs).[1,3,5] To break the limitation of "memory wall," great efforts have been paid to develop ultrafast nonvolatile memory with ultrahigh operation speed, long-term retention, and low power consumption.[6–13] For instance, quasi-nonvolatile memories based on a semi-floating-gate architecture were proposed recently,[3,14–16] which can fill the timescale gap between volatile and nonvolatile memories. However, the retention time of these quasi-nonvolatile memories are still limited (<100 s), and a relatively high gate voltage is required. Thus far, ultrafast nonvolatile memory with nanosecond-timescale operation speed and long-term retention is still unavailable.

Novel device structures and new materials are required to develop ultrafast nonvolatile memory. 2D materials with favorable properties provide an ideal platform for the development of next-generation electronics,[17–20] and various memory devices based on 2D materials have been developed.[6,10,21–24] Semi-floating-gate architecture based on 2D van der Waal heterostructure[3,14,15] is a newly proposed memory technology that can overcome the slow operation speed of conventional floating-gate memories by the direct injection of charges through a p–n junction into the floating gate beyond the Fowler–Nordheim tunneling mechanism. Unfortunately, these devices suffer an inevitable junction leakage of the charges in the floating gate, which leads to a limited retention time, and thus frequent refresh operations are still required. Given that some charge-trapping materials in nonvolatile memories can trap charges for quite a long time,[25–29] it is possible to prevent the leakage of charges by using a charge-trapping material as the charge-trapping layer. In our recent work, long-term retention has been demonstrated by a device based on graphdiyne/graphene (GDY/Gr) heterostructure, where holes are trapped in GDY for over 5000 s.[30,31] By integrating charge-trapping material into the semi-floating-gate memory, there is great potential for significantly improving the retention characteristics of the memory while maintaining its ultrahigh operation speed.

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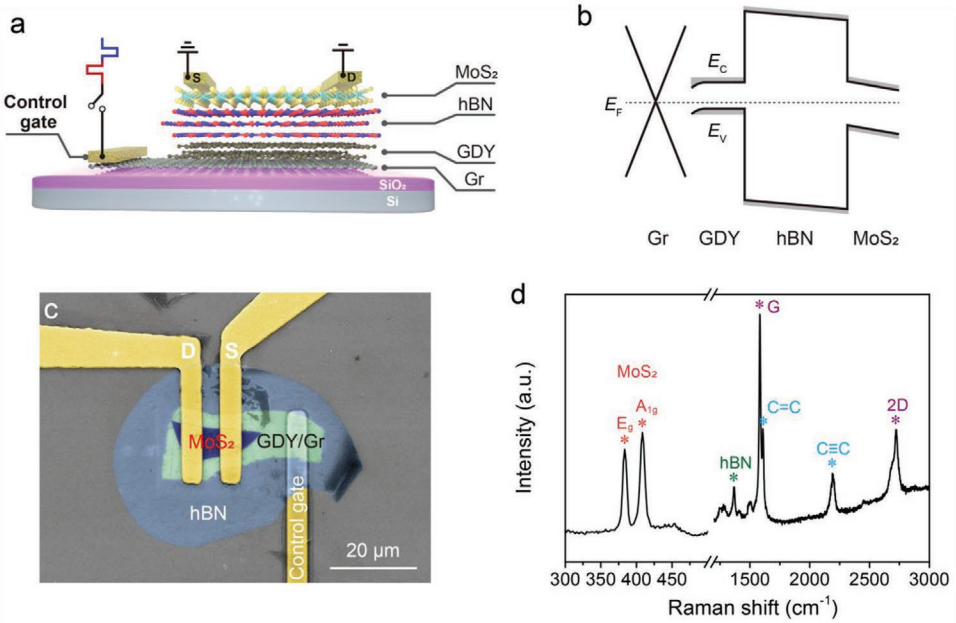

Figure 1. Structure and characterization of the ultrafast nonvolatile memory based on MoS_2/hBN/GDY/Gr heterostructure. a) Schematic of the 2D memory device. The 2D semiconductor MoS_2 acts as the channel and GDY is used as the charge-trapping layer. b) Band diagrams of the device at thermal equilibrium. E_C, E_V, and E_F represent the conduction band, valence band, and Fermi level, respectively. c) False-colored SEM image of the memory device. "D" and "S" represent the drain and source electrodes. d) Raman spectrum of the MoS_2/hBN/GDY/Gr vertical heterostructure. The corresponding Raman bands of MoS_2, hBN, GDY, and graphene are marked by the asterisks with colors of orange, green, cyan, and purple.

Here, we develop an ultrafast nonvolatile memory based on 2D van der Waals heterostructure. This memory device uses GDY as the charge-trapping layer, which is directly connected to the control gate (graphene). Charges are directly injected into the GDY layer through the GDY/Gr junction in an ultrashort time and can be persistently trapped by the trapping sites in GDY. As a result, an ultrahigh writing speed (≈8 ns), a low writing voltage (30 mV), and a long retention time (over 10^4 s) have been demonstrated by this device. In addition, the high on/off ratio of 10^6 enables the achievement of 6 discrete storage levels, indicating its potential for multibit storage. This device fills the blank of ultrafast nonvolatile memory technology.

2. Results and Discussion

Figure 1a schematically illustrates the structure of the ultrafast nonvolatile memory based on MoS_2/hexagonal boron nitride (hBN)/GDY/Gr heterostructure. A multilayer MoS_2 with a thickness of 3 nm acts as the channel, while a thick hBN film (20 nm) serves as the blocking layer. GDY is used as the charge-trapping layer, and graphene acts as the control gate of the device. MoS_2, hBN, and graphene were fabricated by mechanical exfoliation, and GDY was synthesized via a solution phase van der Waal epitaxial approach on surface of graphene.[32] Details for the synthesis of GDY and device fabrication are described in Note S1 (Supporting Information). Figure 1c shows the scanning electron microscope (SEM) image of the fabricated device on SiO_2/Si substrate. The control-gate electrode is connected to graphene, and the source and drain electrodes are overlapped on the MoS_2 channel. The heavily p-doped Si substrate is used as the back gate, with 285 nm SiO_2 as gate dielectric. It is worth noting that in this work, the back gate is mainly used to estimate the trapped charges in GDY and perform control experiments. The back gate is floated during the write and erase operations. Figure 1d presents the Raman spectrum of the MoS_2/hBN/GDY/Gr vertical heterostructure. The Raman bands at 383.5 and 408.3 cm^{-1} correspond to the E_g and A_{1g} bands of MoS_2,[33] while the Raman band at 1365.2 cm^{-1} is attributed to the hBN.[34] The Raman G and 2D bands of graphene are marked at 1582.6 and 2719.8 cm^{-1}, respectively, while the Raman bands at 1608.8 and 2195.5 cm^{-1} are ascribed to the sp^2 and sp hybridization of GDY.[32] The atomic force microscopy and Raman mapping images of the device are illustrated in Figures S4 and S5 (Supporting Information).

In conventional floating-gate memories, the inefficient tunneling of charges through the blocking layer leads to a slow operation speed. To achieve an ultrahigh writing speed, our device uses GDY as the charge-trapping layer, which is directly connected to the graphene control gate, and thus the charges are directly injected into the charge-trapping layer through the GDY/Gr junction driven by the control-gate bias (V_{CG}). The Fermi levels of pristine graphene and GDY are 4.6 and 5.06 eV (Figure S6, Supporting Information), respectively. The work function mismatch between GDY and graphene results in a downward band bending at the GDY/Gr interface, facilitating the transport of holes from graphene to GDY. It has been demonstrated that the charge transport in 2D van der Waals heterojunctions takes place within femtoseconds since the charges only need to move less than several nanometers vertically for the atomically thin heterostructures.[35] In addition, the highly π-conjugated structures of both graphene and GDY[36] facilitate

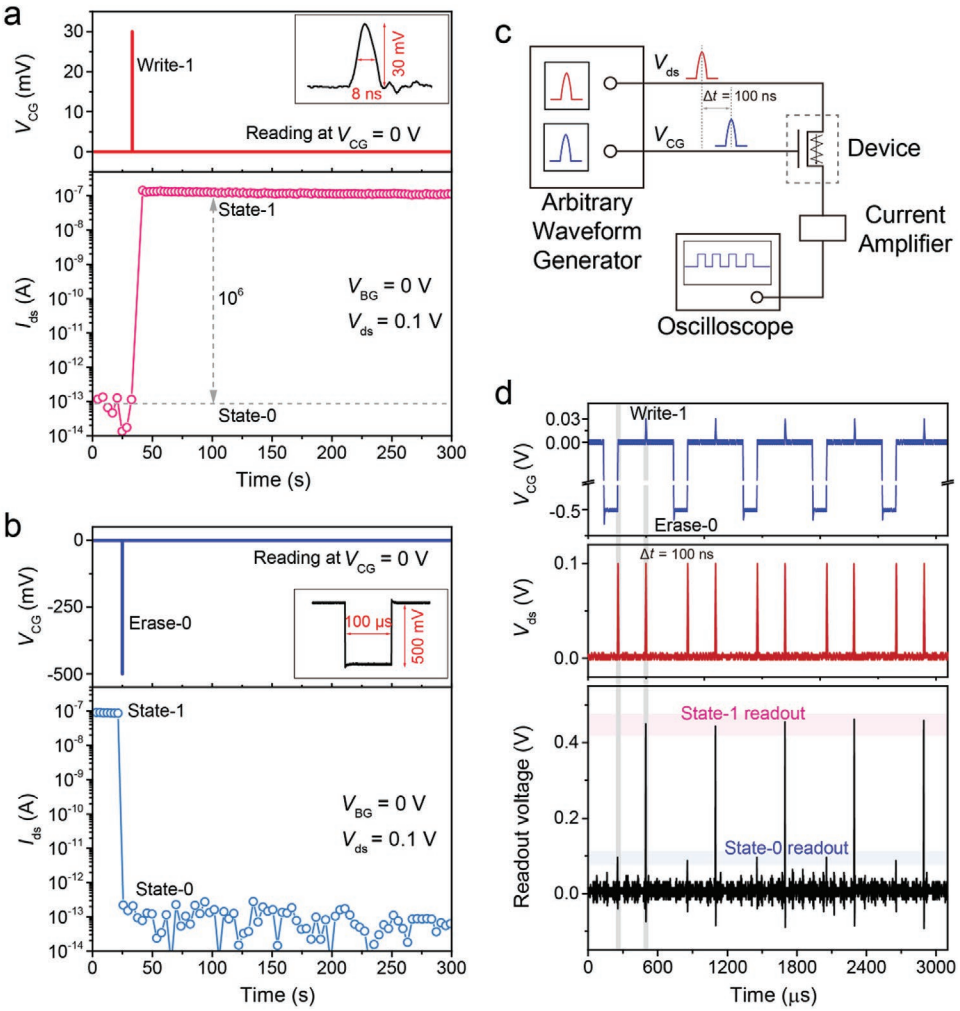

Figure 2. Ultrafast writing/erasing and readout operations of the nonvolatile memory device. a) Write-1 operation followed by Read-1 operation. An ultrafast V_{CG} pulse with FWHM of 8 ns and voltage of +30 mV was used to program the memory from State-0 to State-1. The ratio of State-1 and State-0 is 10^6. The following Read-1 operation was carried out with V_{ds} = 0.1 V and V_{CG} = 0 V. The inset in the top panel is the real V_{CG} signal applied to the control gate measured by the oscilloscope. b) Erase-0 operation and the following Read-0 operation. A –0.5 V V_{CG} pulse with width of 100 µs was used to erase the device from State-1 to State-0. The Read-0 operation was performed at V_{ds} = 0.1 V and V_{CG} = 0 V. c) Circuit diagram for high-speed readout measurement. An arbitrary waveform generator was used to generate V_{CG} and V_{ds} pulses with controlled delay (Δt) applied to the control-gate and drain electrodes, while a current amplifier and an oscilloscope were used to convert the output current signals into voltage signals and read out these signals, respectively. d) The applied V_{CG} (blue) and V_{ds} (red) pulses with a delay of 100 ns, and the corresponding readout voltage signals (black). All input and output signals in (d) were measured by an oscilloscope.

the charge transfer between the adjacent graphene and GDY layers, endowing the GDY/Gr vertical heterostructure with an ultrafast charge-transport speed. Thus, the injection of holes from graphene to GDY through GDY/Gr heterojunction can complete in an ultrashort time less than nanoseconds, enabling the ultrahigh writing speed for our device. According to the band structures and Fermi levels of graphene, GDY, hBN, and MoS_2 (Figures S6–S9, Supporting Information),[12,24] we can infer the band diagrams of the device at thermal equilibrium, as shown in Figure 1b. Owing to the work-function difference between MoS_2 and GDY, the multilayer MoS_2 layer is initially depleted of mobile carriers.[37] The well-engineered band offset of the GDY/Gr heterojunction, as well as the excellent charge-trapping capability of GDY[31,38–40] restrict the injected holes in the GDY layer, resulting in a long retention time.

The writing and erasing operations of the ultrafast nonvolatile memory were carried out by applying positive and negative control-gate (V_{CG}) pulses, respectively. **Figure 2**a shows the ultrafast writing operation of the nonvolatile memory with an ultralow positive V_{CG} pulse. An 8 ns full width at half maximum (FWHM) V_{CG} pulse with amplitude as low as 30 mV (the inset in Figure 2a) was used to program the memory from State-0 (10^{-13} A) to State-1 (10^{-7} A), with an on/off ratio of 10^6. When the ultrafast positive V_{CG} pulse was applied, a large amount of holes were directly injected into the GDY charge-trapping layer through the GDY/Gr heterojunction rapidly. After the Write-1 operation, a readout operation Read-1 was performed by

applying a drain voltage V_{ds} of 0.1 V at V_{CG} = 0 V. The readout channel current was measured as 10^{-7} A, indicating that the memory was programmed to State-1. For the erasing operation, a negative V_{CG} pulse with a relatively higher amplitude and longer duration is required due to the asymmetry band offset of the GDY/Gr heterojunction. As shown in Figure 2b, a negative V_{CG} pulse of −0.5 V with a width of 100 µs was applied to the device, resulting in the erasing of the device from State-1 back to State-0. The readout operation Read-0 was also monitored with V_{ds} = 0.1 V. It is worth noting that the back gate was floated during the whole writing/erasing and readout operations here.

In addition to the ultrafast writing speed, this memory device also features a nanosecond-timescale readout speed, which is important for practical applications. As shown in Figure S10 (Supporting Information), V_{ds} pulses with a FWHM of 30 ns generated by an arbitrary waveform generator were applied to the drain electrode of the device, and the readout signals by an oscilloscope were quite distinct for the device at State-1 and State-0. Furthermore, the readout operations were performed after the Write-1 and Erase-0 operations with a delay (Δt) of 100 ns. The delay between the V_{CG} and V_{ds} pulses was controlled by the arbitrary waveform generator (Figure 2c). As shown in Figure 2d, the channel currents of the device at State-0 and State-1 can be distinguished by the oscilloscope. That is, the data can be read out within 100 ns after the writing and erasing operations. It is worth noting that the delay time of 100 ns is the smallest time that the instrument can control accurately, and thus the device also features a nanosecond-timescale readout speed.

Figure S11 (Supporting Information) shows the transfer curve of the device by applying sweeping gate voltage to the graphene control gate. The subthreshold swing (SS) is calculated as 94 mV dec^{-1} for V_{ds} = 0.1 V. The SS is given by[37]

$$SS = \frac{kT}{q}\ln(10)\times\left(1+\frac{C_S+C_{it}}{C_{ox}}\right) \quad (1)$$

where C_S is the depletion capacitance of MoS_2, C_{it} is the MoS_2/hBN interface state capacitance owing to the interface traps, and C_{ox} is the gate capacitance. The depletion capacitance of MoS_2 (C_S) is negligible in the deep-subthreshold region. Since hBN features an atomically smooth and defect-free surface, the interface trap density is very low, resulting in a small C_{it}. In addition, the relatively thin thickness of hBN results in a large C_{ox} according to $C_{ox} = \varepsilon_{ox}\varepsilon_0/d$. Thus, the device features a small SS which is close to the theoretical minimum value at room temperature (≈60 mV dec^{-1}). Since the back gate is floated during the measurement, charges are hard to tunnel through the thick SiO_2 (285 nm) to the back gate driven by such a small V_{CG} voltage. Thus, SiO_2/Si can be regarded as a substrate of the device, and the capacitance of SiO_2 is not considered here. The SS is an important parameter to estimate the switching speed of the device between the off and on states. Such a small SS indicates that the device features a relatively high intrinsic operation speed, and the channel current can be read out within an ultrashort time (nanosecond timescale) after the writing/erasing operations.

The ultrahigh operation speed of the device is mainly attributed to the direct injection of charges into the charge trapping layer through the GDY/Gr heterojunction, instead of the inefficient tunneling through the blocking layer. Control experiments were performed by using back-gate voltage (V_{BG}) and bias voltage (V_{ds}) pulses to program the device, respectively. Just like a conventional floating-gate memory, the device can be programmed and erased by a negative and positive V_{BG} pulses with large amplitude and long duration (±20 V, 1 s) (Figure S12, Supporting Information). In addition to V_{BG} pulse, V_{ds} pulses have also been demonstrated to drive the charge tunneling through the blocking layer via Fowler–Nordheim tunneling.[12,39] However, just as shown in Figure S13 (Supporting Information), a relatively large voltage and long duration are also required for the bias-voltage mode.

To estimate the density of the trapped holes in GDY, the transfer curves of the memory device at State-0 and State-1 were measured. As shown in **Figure 3**a, there is an obvious left shift of the threshold voltage of the MoS_2 channel after writing operation. As shown in Figure S14 (Supporting Information), the hysteresis of the double sweep transfer curve driven by back-gate voltage V_{BG} is quite small, which indicates that the charge tunneling through thick hBN blocking layer is negligible. Thus, we can conclude that the shift of the threshold voltage is induced by the trapped holes in the GDY charge-trapping layer. The density of the trapped holes was calculated as 0.95×10^{12} cm^{-2}, using the formula[41,42]

$$D = (\Delta V_{th}\times C_{total})/q \quad (2)$$

where ΔV_{th} is the shift of the threshold voltage and q is the electron charge. C_{total} is the total capacitance between the MoS_2 channel and the back gate, which can be calculated by the equations[23,41]

$$\frac{1}{C_{total}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{hBN}} \quad (3)$$

and

$$C = \varepsilon_0\varepsilon_r/d \quad (4)$$

where ε_0 and ε_r are the vacuum permittivity and relative dielectric constant (3.9 for SiO_2 and 3.5 for hBN), respectively, while d is the thickness. Figure 3b presents the output curves of the device at State-0 and State-1, which were measured at V_{CG} = 0 V and V_{BG} = 0 V. The readout operation is nondestructive to the storage performance of the device duo to the thick hBN blocking layer.

Multilevel storage can be achieved by controlling the trapped charge density in GDY. Here, the injected holes are controlled by the voltage of the applied V_{CG} pulse. Figure 3c shows the dynamic response of the memory device after the Write-1 operation by applying an ultrafast V_{CG} pulse (8 ns) with amplitude decreasing from 30 to 2 mV. As shown in Figure 3d, the channel current of the memory after Write-1 operation decreases with the decrease of the V_{CG} voltage. The on/off ratio is still ≈10^2 even though the amplitude of the V_{CG} pulse is as low as 2 mV. Table S1 (Supporting Information) summarizes the operation voltage of the memory devices, which always require a relatively high voltage for writing operation. By contrast, our memory device features an ultralow writing voltage, which can significantly decrease the power consumption. The voltage-dependent

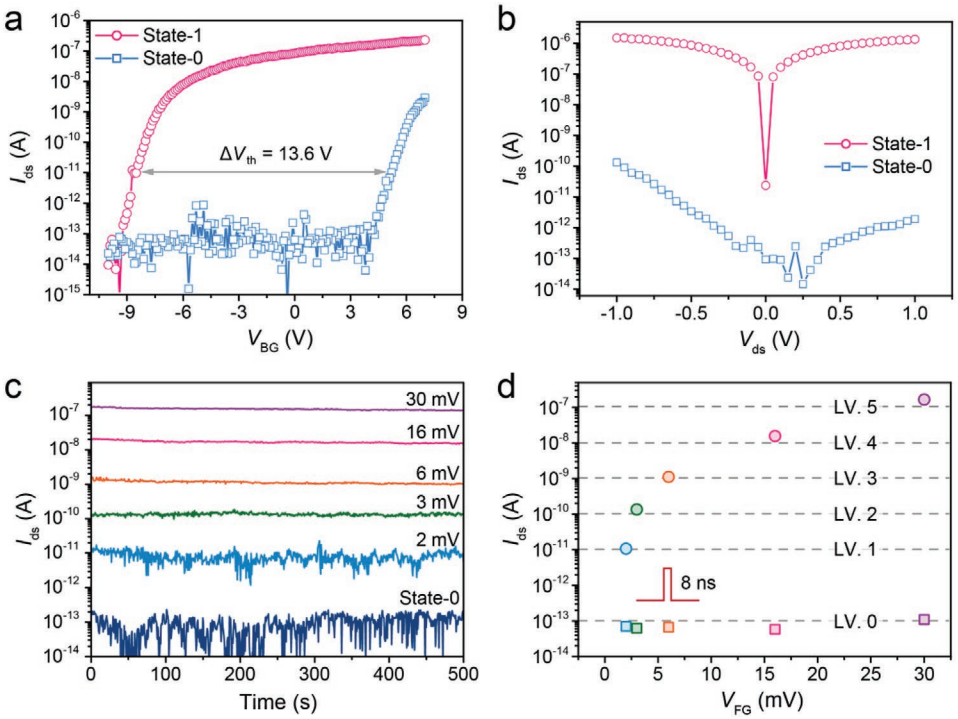

Figure 3. Voltage-dependent Write-1 operation for multilevel storage. a) Transfer curves of the memory device measured at State-1 (red) and State-0 (blue), respectively. V_{ds} = 0.1 V, V_{CG} = 0 V. b) Output curves of the device at State-1 and State-0 measured with V_{CG} = V_{BG} = 0 V. c) The readout currents of the device at State-0 and State-1 after Write-1 operation with different amplitude of V_{CG} pulses. The FWHM of the V_{CG} pulses are 8 ns and V_{ds} = 0.1 V. d) Voltage-dependent current levels of the memory after Write-1 operation with 6 discrete storage levels.

current levels of the memory after Write-1 operation make it possible to achieve multibit storage, which can store more than one-bit data in a single unit. Here, 6 discrete storage levels have been demonstrated, significantly increasing the storage capability of the memory.

The endurance and retention characteristics are crucial for memory devices. Given the device could be programmed by a quite small voltage, which makes it easy to be disturbed by voltage fluctuation and environment noise, the device should be well encapsulated for a robust stability. **Figure 4**a presents the switching operation of the memory device between State-0 and State-1 by applying alternating positive and negative V_{CG} pulses. The channel currents of the device at State-0 and State-1 are almost unchanged and maintain the on/off ratio up to 10^6 for 1000 writing/erasing cycles (Figure 4b), demonstrating the excellent endurance of the memory device. Furthermore, the retention characteristics of the device at State-1 and State-0 were also investigated. The channel currents after Write-1 and Erase-0 operations were measured by applying a drain voltage of 0.1 V at V_{CG} = 0 V. As shown in Figure 4c, a long retention time over 10^4 s has been demonstrated by this memory device, which is comparable to that of the nonvolatile memory devices based on 2D materials (Table S1, Supporting Information). The leakage of the trapped holes in GDY is significantly suppressed, which can be attributed to the excellent charge-trapping capability of GDY,[31,38–40] as well as the potential well formed by the GDY/Gr heterojunction and hBN barrier. Here, we would like to clarify that a thick hBN is not essential for the long retention time of the device, especially considering such a thick hBN film is unfriendly to real application. As shown in Figure S15 (Supporting Information), memory device with a 9 nm thick hBN blocking layer exhibits comparable retention characteristics. To further improve the robustness of the device to resist voltage fluctuation and environment noise, we will appropriately increase the threshold of the write voltage by optimizing the band offsets of the heterostructure.

The GDY charge-trapping layer is crucial for the ultrahigh writing speed and long retention time of the memory device. Control experiments were carried out by measuring the storage performance of the memory device without GDY charge-trapping layer. As shown in Figure S16 (Supporting Information), a device with a structure of MoS_2/hBN/Gr without GDY charge-trapping layer was fabricated. The absence of the GDY layer led to the failure of charge storage in the control gate by applying V_{CG} pulses. As a result, this device did not exhibit any obvious memory characteristics after V_{CG} pulses (±1 V, 1 s).

Table S1 (Supporting Information) summarizes the parameters of the reported nonvolatile and quasi-nonvolatile memories based on 2D materials and other material systems. In comparison with these memories, the most significant advantages of our ultrafast nonvolatile memory are its ultrahigh writing speed, long retention time, and low operation voltage. Figure 4d summarizes the operation speed and retention time of these devices. The volatile and quasi-nonvolatile memories feature an ultrahigh operation speed (on nanosecond timescale) but a limited retention time, whereas the nonvolatile memory devices exhibit a robust retention ability but a relatively slow speed (over 100 µs). The area nearby the ideal memory that

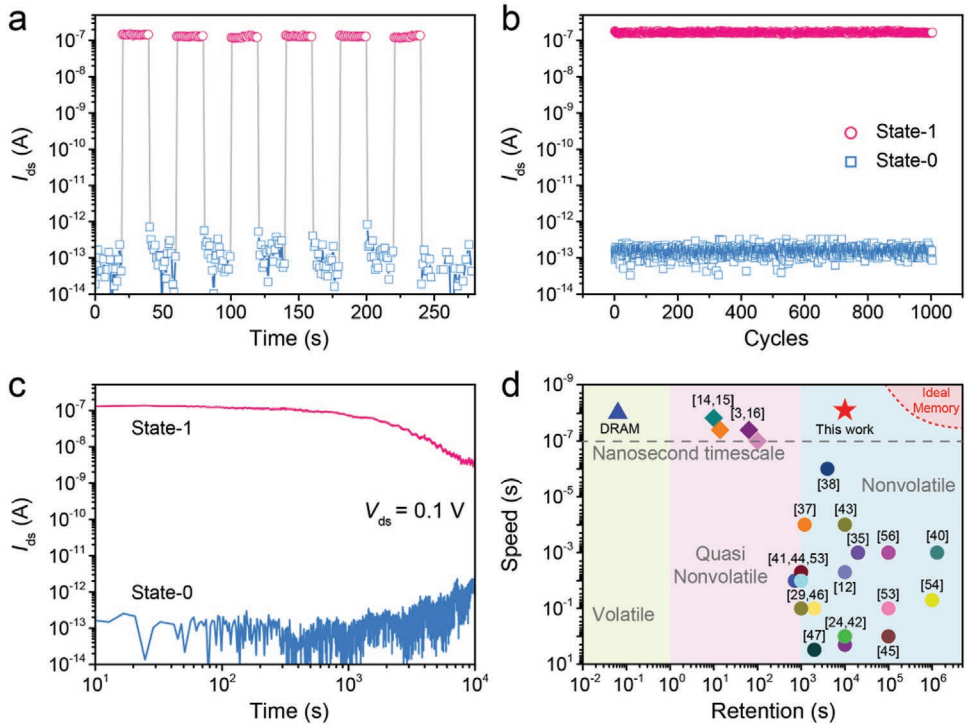

Figure 4. Endurance and retention characteristics of the ultrafast nonvolatile memory. a) Switching of the device between State-0 and State-1 by applying alternating positive (+30 mV, 8 ns) and negative (–0.5 V, 100 µs) V_{CG} pulses. V_{ds} = 0.1 V. b) Variation of the State-0 and State-1 currents from the initial to 1000 writing/erasing cycles during the endurance test. c) Retention characteristics of the memory device after Write-1 and Erase-0 operations. The currents are measured at V_{ds} = 0.1 V and $V_{CG} = V_{BG}$ = 0 V. d) Comparison of the operation speed and retention time of the reported volatile, nonvolatile, and quasi-nonvolatile memories.

combines ultrahigh operation speed and long retention time is still blank. Our memory device is located closest to the ideal memory, filling the blank of ultrafast nonvolatile memory technology. Its long retention time (over 10^4 s) is 1.5 × 10^5 times and 100 times longer than that of DRAMs and the reported quasi-nonvolatile memories, respectively.[3,14–16] The ultrahigh operation speed (8 ns) of our memory is ≈10^4 times and 10^6 times faster than that of the commercial NAND/NOR flash memories and the nonvolatile memories based on 2D materials, respectively.[5,23,43,44] Given the retention time of the device (10^4 s) is still far from the requirement of memory applications, in which more than 10 years' retention is favorable, one of the potential applications of the memory device is RAMs. For conventional DRAMs with millisecond-timescale retention time, frequent refresh operations are required to keep stored data, which lead to an increased power consumption. By contrast, the long refresh time (10^4 s) of our memory device can significantly decrease the refresh frequency and power consumption of the RAMs.

Figure 5 illustrates the band diagrams and charge-flow illustrations of the device at different operations. For Write-1 operation, a positive V_{CG} pulse is applied to the control gate, which would induce the drop of the graphene Fermi level and promote the injection of holes to the GDY layer through the GDY/Gr heterojunction (Figure 5a). As a result, a 2D electron gas forms in the MoS_2 layer closest to the hBN film,[37] and thus the device switches from State-0 to State-1. The direct injection of holes through GDY/Gr heterojunction results in the significantly improved writing speed on nanosecond timescale. It is worth noting that charges tunneling through the thick hBN blocking layer under such a small voltage and short time can be negligible. After the ultrafast V_{CF} pulse, the injected holes are persistently restricted in the GDY layer by the trapping sites in GDY and the potential well formed by the GDY/Gr interface and the hBN barrier (Figure 5b). Thus, the leakage of the trapped holes is significantly suppressed, resulting in a long retention time at Read-1 operation. The Erase-0 operation is illustrated in Figure 5c, where a negative V_{CG} pulse applied to the control gate would elevate the Fermi level of graphene, and thus facilitates the extraction of the trapped holes from GDY back to graphene. Due to the asymmetric band offset of the GDY/Gr heterojunction, a V_{CG} pulse with relatively large amplitude and width is required for Erase-0 operation to overcome the potential barrier. After erasing operation, the trapped holes in GDY are released, and as a result, the MoS_2 channel current switches from State-1 back to State-0 (Figure 5d).

Although the erasing speed of our memory device exceeds the reported nonvolatile memory devices based on 2D materials, it is still inferior in comparison with the ultrahigh writing speed due to the specific band offset of the GDY/Gr heterostructure and the excellent charge-trapping capability of GDY. Especially, the charge-trapping sites in GDY can be regarded as the potential wells, and thus a relatively larger voltage and longer duration

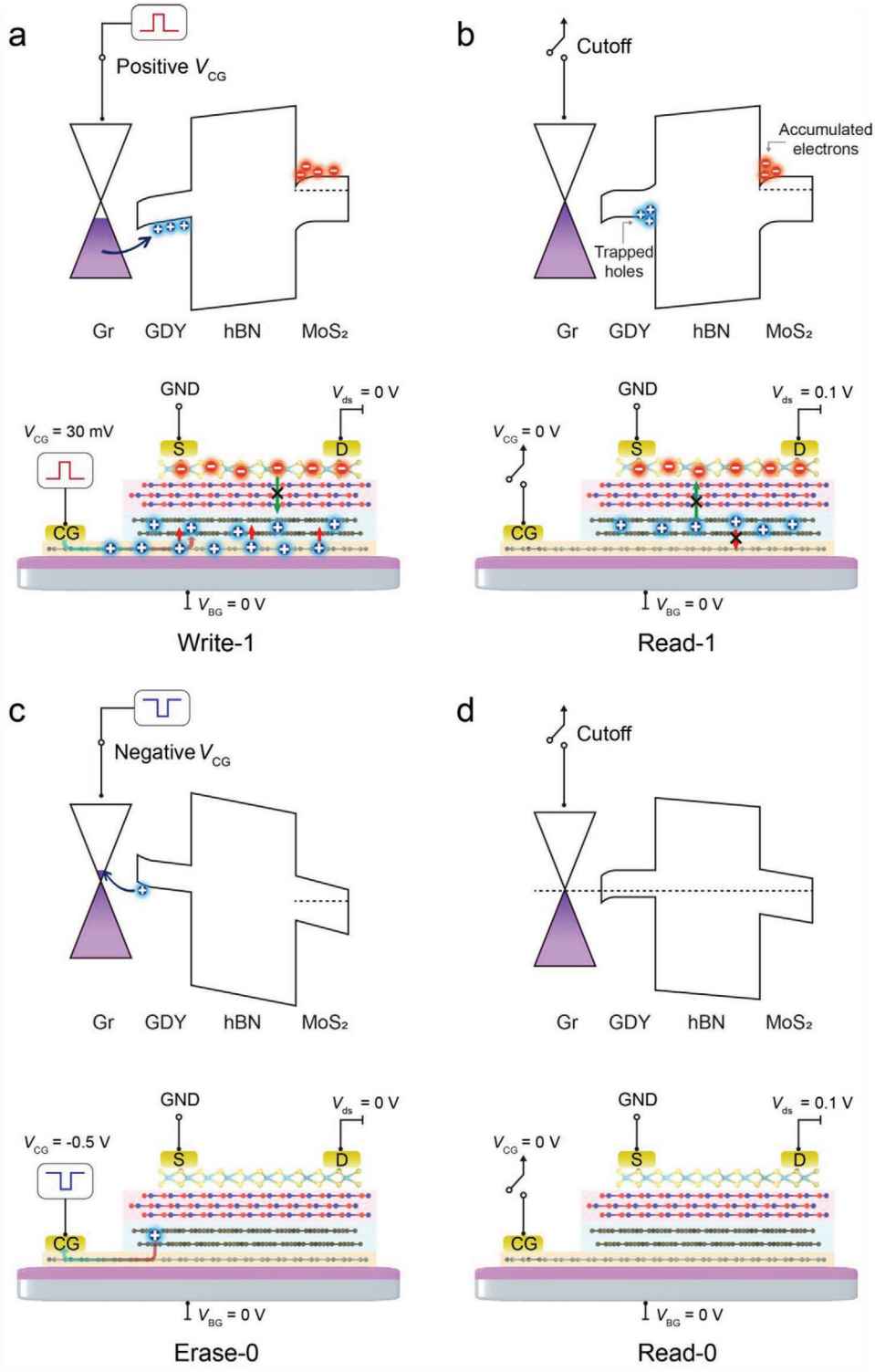

Figure 5. Operation mechanisms of the memory device. a–d) Band diagrams and charge transport of the device at (a) Write-1, (b) Read-1, (c) Erase-0, and (d) Read-0 operations. The blue balls and arrows illustrate the holes and the hole flow direction, and the red balls indicate the electrons.

are required to extract the trapped holes from the deep potential wells of the charge-trapping sites, which is adverse for erase operation. Next, we will seek for more appropriate charge-trapping materials to construct ultrafast nonvolatile memories with symmetric ultrahigh writing and erasing speeds. In addition, in our following works, we will further optimize the device structure and band offset of the heterostructure to achieve a more robust device with much longer retention time.

3. Conclusion

In conclusion, we have proposed an ultrafast nonvolatile memory based on MoS_2/hBN/GDY/Gr vertical heterostructure. The ultrafast writing speed (8 ns) and low operation voltage (30 mV) are attributed to the direct injection of charges into the charge-trapping layer, while the long retention time (over 10^4 s) is ascribed to the band-engineered heterostructure and excellent charge-trapping capability of GDY, which can significantly suppress the leakage of the trapped charges in GDY. Moreover, the high on/off ratio (10^6) of the device enables the achievement of multibit storage with 6 discrete storage levels, which improves the storage density of the memory. This device combines the advantages of the ultrafast writing speed for volatile memory and long retention time for nonvolatile, filling the blank of ultrafast nonvolatile memory technology.

4. Experimental Section

Device Measurements: The performance of the memory was measured in a probe station connected to a semiconductor device parameter analyzer (Keithley 4200A-SCS) and an arbitrary waveform generator (RIGOL DG4202). The DC drain and back-gate signals were generated by the source/monitor units of Keithley 4200A, and the V_{CG} pulses with different widths and amplitudes were generated by the arbitrary waveform generator. The current signals were measured by the Keithley 4200A equipped with preamplifiers. A current amplifier (FEMTO DHPCA-100) was used to convert the output current signals into voltage signals and an oscilloscope (RIGOL DS2302A) was used to read these voltage signals during the ultrafast readout measurements. Before measurement, the device was pre-erased to the off state. All the measurements were carried out at room temperature in vacuum.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

charge trapping, direct charge injection, graphdiyne, multibit storage, ultrafast nonvolatile memories

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